



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1430
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,814	02/27/2002	Joseph Francis Mann	01AB162	6548
7590	09/14/2005		EXAMINER	
Ms. Susan M. Donahue Rockwell Automation, 704-P 1202 South Second Street Milwaukee, WI 53204			CHEN, TSE W	
			ART UNIT	PAPER NUMBER
			2116	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/083,814	MANN ET AL.
	Examiner Tse Chen	Art Unit 2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 June 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-21 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Remarks dated June 9, 2005.
2. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kao et al., US Patent 4720812, hereinafter Kao.
5. In re claim 1, Kao discloses an integrated processor system [fig.3] comprising interconnected:

- Processing unit [50] for performing arithmetic and logical operations.
- Non-volatile boot memory [58] holding a bootstrap program.
- At least one internal system storage structure selected from the group consisting of caches [56], buffers [64], and registers [col.3, ll.42-44].
- Wherein the processing unit executes at least a portion of the bootstrap program using an internal system storage structure for temporary storage without access to external memory [40] [col.3, ll.4-22; col.3, l.65 – col.4, l.33; col.5, l.61 – col.6, l.18; execute bootstrap with internal memory without accessing an external magnetic disk].

Art Unit: 2116

6. As to claims 2 and 13, Kao discloses, including interface circuits [inherently some interface circuit in the broadest interpretation is needed for communication] for communicating electrical signals [i/o control signals] with non-memory external devices [peripheral devices] [col.6, ll.19-40].

7. In re claim 12, Kao discloses each and every limitation of the claim, as discussed above in reference to claim 1. Kao discloses the integrated processor system; therefore, Kao discloses the method of operating the integrated processor system.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3-7, 10-11, 14-17, 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao as applied to claim 1 above, and further in view of Fullam et al., US Patent 5802550, hereinafter Fullam.

10. In re claims 3 and 14, Kao taught each and every limitation of the claim, as discussed above in reference to claim 1. Kao discloses the integrated processor system further including a memory interface [inherently some interface in the broadest interpretation is needed for communication] for communicating with external memory [40] and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of external memory data [col.3, ll.4-22]. Kao did not disclose the acquisition of external memory setup data required for the memory interface to initiate communication with external memory.

11. Fullam discloses an integrated processor system [fig.3] including a memory interface [56] for communicating with external memory 58, 64] and wherein the processing unit [52] executes at least a portion of the bootstrap program [boot process] to provide for the acquisition of external memory setup data [configuration data] required for the memory interface to initiate communication with external memory [col.7, ll.39-50].

12. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao and Fullam before him at the time the invention was made, to modify the integrated processor system taught by Kao to include the teachings of Fullam, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase flexibility by allowing the processing unit to interact with number of different external memory types [Fullam: col.1, l.65 – col.2, l.32].

13. As to claims 4 and 15, Fullam discloses, including: a network interface and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data through a network connection [col.7, ll.39-50; configuration data stored in external 64 accessed through network].

14. As to claims 5 and 16, Fullam discloses, wherein the external memory includes non-volatile memory [64] and volatile memory [58] and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data for the external volatile memory from the external non-volatile memory [col.3, ll.59-63; col.7, ll.39-50].

15. As to claim 6, Fullam discloses, comprising wherein the external non-volatile memory is flash memory [col.7, ll.41-42].

Art Unit: 2116

16. As to claims 7 and 17, Fullam discloses, wherein the processing unit includes an address translation table mapping processing unit addresses to addresses of the external memory [col.6, l.39 – col.7, l.10] and Kao discloses, wherein the processing unit executes at least a portion of the bootstrap program to make a temporary address translation table in a buffer memory [col.7, ll.37-42] so as to make the cache memory [56] available for temporary storage [col.9, ll.5-42].

17. As to claims 10 and 20, Fullam discloses, wherein the processing unit further executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] and then to execute a program contained in external memory [col.1, ll.25-50; col.7, l.38 – col.8, l.19].

18. As to claims 11 and 21, Fullam discloses, wherein the memory setup data is selected from the group consisting of: memory type as static or dynamic, memory speed, memory size, memory parity, and memory timing [col.3, ll.47-58; col.7, ll.11-26; col.9, ll.5-7].

19. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao as applied to claim 1 above, and further in view of Devereux., US Patent 6671779.

20. In re claims 8 and 18, Kao taught each and every limitation of the claim, as discussed above in reference to claim 1. Kao discloses the integrated processor system wherein the system storage structure is a cache memory [56] and wherein the processing unit executes at least a portion of the bootstrap program to read arbitrary data into the cache memory [col.3, ll.42-44; col.9, ll.21-42]. Kao did not disclose locking the cache memory against further reading or writing to external memory.

21. Devereux discloses an integrated processor system [fig.3] wherein the system storage structure is a cache memory [30'] and wherein the processing unit [10] executes at least a portion

Art Unit: 2116

of the bootstrap program to read arbitrary data [data values for interrupts] into the cache memory and then to lock the cache memory against further reading or writing to external memory [80] so that it may be used as variable storage for further execution of the bootstrap program [col.7, ll.36-49].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao and Devereux before him at the time the invention was made, to modify the integrated processor system taught by Kao to include the teachings of Devereux, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides speed benefits without data corruption [Devereux: col.7, ll.36-49].

23. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao and Fullam as applied to claim 3 above, and further in view of Little et al., US Patent 6272637, hereinafter Little.

24. In re claims 9 and 19, Kao and Fullam taught each and every limitation of the claim, as discussed above in reference to claim 3. Fullam discloses wherein the processing unit executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] [col.1, ll.25-50; col.7, l.38 – col.8, l.19]. Kao and Fullam did not disclose explicitly loading additional programs for execution into external memory.

25. Little discloses an integrated processor system [fig.3] wherein the processing unit loads additional programs for execution into external memory [130] [col.5, ll.39-51].

26. It would have been obvious to one of ordinary skill in the art, having the teachings of Kao, Fullam and Little before him at the time the invention was made, to modify the integrated

Art Unit: 2116

processor system taught by Kao and Fullam to include the teachings of Little, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides secured processing of information [Little: col.1, ll.39-59].

Allowable Subject Matter

27. The indicated allowability of claims 5, 8, 16, and 18 are withdrawn in view of the newly discovered reference(s) to Devereux and reconsideration of Fullam. Rejections based on the new grounds are discussed above.

Response to Arguments

28. Applicant's arguments filed June 9, 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
September 12, 2005



LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100